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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/824,549	04/02/2001	Yoshimitsu Nakashima	70840-55652	9425	
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Dike, Bronstein, Roberts & Cushman			EXAMINER		
EDWARDS &	-		HARRINGTON, ALICIA M		
130 Water Stree Boston, MA 02	-		ART UNIT	PAPER NUMBER	
,			2873		
			DATE MAILED: 06/27/2002	DATE MAILED: 06/27/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. Application Application	•		\mathcal{M}			
Examiner Art Unit Alcia M Harrington 2873 273 273 273 274 274 274 275 2		Application No.	Applicant(s)			
Alciae M Harrington 2873 - The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. He may be a subject to reply specified above is less than thirty (30) days, are play within the standary minimum of thirty (30) days with be considered timely. He period for reply specified above is less than thirty (30) days, and event, however, may a reply be timely filled and read to 30 (s) MONTHS from the mailing date of this communication. He period for reply specified above is less than thirty (30) days, and event, however, may a reply be timely filled and read to 30 (s) MONTHS from the mailing date of this communication. He period for reply specified above is less than they (30) days, and event, however, may a reply be timely filled and reply and the period of the communication. He period for reply specified above is less than they are subjected to the communication, even if timely filled, may reduce any common produce any reply received by the Office later than three monities date fills mailing date of this communication, even if timely filled, may reduce any common produce any common produce any reply reduced any reduced an	Office Action Summan					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address — Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ③ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extendings of time may be available under the provisions of 37 CRF. 1.38(a). In no event, however, may a reply be timely filled at the provision of the provisions of 37 CRF. 1.38(a). In no event, however, may a reply be timely filled at the period for reply aspected above, the mainting address present of allow present of a second or present of the communication. Event fill the present of the communication to become ABANCOIED (95 U.S.C. § 133). **Responsive to communication(s) filed on 4/02/01. **Status** 1) Sesponsive to communication (s) filed on 4/02/01. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under £x parte Quayle, 1935 C.D. 11, 453 O.G. 213. **Disposition of Claims** 4) Claim(s) 1.2 Is/are pending in the application. 4a) Of the above claim(s) is are allowed. 5) Claim(s) is/are allowed. 6) Claim(s) is/are allowed. 6) Claim(s) is/are allowed. 7) Claim(s) is/are allowed. 8) Claim(s) is/are objected to by the Examiner. 10) The drawing(s) filed on 0/2 April 2001 (s/are s. I) accepted or b) objected to by the Examiner. 4) Priority and may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is all paper void by the Examiner. 12) The oath or declaration is objected to by the Examiner. 13) All b) Some *c) None of: 14S Certified copies of the priority documents have been received in Application No	, Office Action Summary	Examiner	Art Unit			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Ederations of time may be available under the provisions of 37 CFR 1.35(s). In no event, however, may a reply be timely filed. Ederations of times may be available under the provisions of 37 CFR 1.35(s). In no event, however, may a reply be timely filed. Ederations of times may be available under the provisions of 37 CFR 1.35(s). In no event, however, may a reply be timely filed. Ederations of times provided above, he maximum statistory period will apply and the statistory minimum of thiny (30) days will be considered timely. Ederation of the specified above, he maximum statistory period will apply and the spire SIX (6) MONTHS from the mailing date of this communication. Failure to report which has a for advantage prior of the mailing date of this communication, when it timely filed, may reflece any summarial plants term adjustment. See 37 CFR 1.704(s). Status 1) Responsive to communication(s) filed on 4/02/01. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 c.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-2 is/are pending in the application. 4) Claim(s) 1-2 is/are pending in the application. 4) Claim(s) 1-2 is/are allowed. 6) Claim(s) 1-3 is/are allowed. 6) Claim(s) 1-3 is/are allowed. 7) Claim(s) 1-3 is/are objected to. 8) Claim(s) 1-3 is/are objected to by the Examiner. Application Papers 9) The proposed drawing correction filed on 1-3 is allowed. 10) The drawing(s) filed on 02 April 2001 is/are: all accepted or b) Disposition of the provision of the priority documents have been received by the Examiner. If approved, corrected drawings are required in reply to this Office action. 12) The oath or declaration is objected to by the Examiner. Priority under 35 U.S.C.	The MAN INC DATE of this security of inch					
THE MAILING DATE OF THIS COMMUNICATION. Edentions of time may be available under the provision of 3 CFR 1.15(6). In no event, however, may a reply be timely filed after SX (8) MONTHS from the mailing date of this communication. It is a start of time may be available under the provision of 3 CFR 1.15(6). In no event, however, may a reply be timely filed after SX (8) MONTHS from the mailing date of this communication. It is a start of reply subject to the mailing date of this communication. Failure to reply visible the set are the time maining date of this communication. Any reply received by the Office sheet than there inmaining date of this communication, even if timely filed, may reduce any size placet term adjustment. See 3 T CFR 1.79(6). Status 1) Responsive to communication(s) filed on 4/02/01. 2a) This action is FINAL. 2b) This action is FINAL. 2c) This action is FINAL. 2c) This action is FINAL. 2c) This action is FINAL. 2d) This acti	•	pears on the cover sheet with the	ne correspondence address			
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DETAILED ACTION

Drawings

Figures 5A-5B and 6A-6F should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A-5B pages 2-7) in view of Park et al (GB 2307344A).

Regarding claim 1, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14), a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture.

However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25) Thus, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

Regarding claim 2, applicant discloses the passivation film is made of silicon nitride based film (see pages 2-4).

Regarding claim 3-4, applicant admitted prior art fails to disclose an embodiment where an insulating film is between the passivation and light shield layer. However, passivation films that comprise several layers are notoriously well known in the art, and the Examiner takes official notice to this fact (and can comprise an insulation layer/silicon nitride layer). Further, Park discloses a BSG and insulation layer of silicon dioxide (17) directly underneath the passivation layer and over the gate layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicants admitted prior art to include an insulation layer between the passivation layer and light-shielding surface, to provide good insulation for semiconductor circuitry.

Regarding claim 5, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture.

However, applicant admitted prior art fails to discloses a planar /flat top surface and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25) Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

In addition, application discloses applying the thin film forming the passivation section by using a CVD technique or the like. Park uses an LPCVD process for planarization of the passivation film. Although, applicant and Park fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and park, to include this process since it is a notoriously well known semiconductor layering process (the Examiner takes official notice to that fact).

Regarding claim 7, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture.

However, applicant admitted prior art fails to disclose a planar /flat top surface, an insulation layer and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Park et al.

In the same field of endeavor, Park discloses the planarization of semiconductor device where the passivation layer 19 is planarized (page 7, lines 22-25). Passivation films that comprise several layers are notoriously well known in the art, and the Examiner takes official notice to this fact (and can comprise an insulation layer/silicon nitride layer). Further, Park discloses a BSG and insulation layer of silicon dioxide (17) directly underneath the passivation layer and over the gate layer. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Park et al. to provide superior insulating property.

In addition, application discloses applying the thin film forming the passivation section by using a CVD technique or the like. Park uses an LPCVD process for planarization of the Application/Control Number: 09/824,549

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passivation film. Although, applicant and Park fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and park, to include this process since it is a notoriously well known semiconductor layering process (the Examiner takes official notice to that fact).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A- pages 2-7) in view of Malazgirt et al (US 4,986,878).

Regarding claim 6, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Malazgirt.

In the same field of endeavor, Malazgirt discloses a method for manufacturing integrated circuits where the passivation film is planarized (col. 4, lines 57-65) and where in the method comprises a forming a thing film used for forming the passivation section, applying an SOG film to the thin film and performing an etch back technique (col. 3, lines 36-56). In a further embodiment, Malazgirt disclose the etch back technique is implemented such that a selective 7 gratio for forming the passivation section is 1 to 1. (See col.-8, lines 65-68 and col. 9, line 1). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant's admitted prior art, as taught by Malazgirt, since it would provide a

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planarized passivation layer and circuit which is protected from ambient conditions and handling.

Regarding claim 8, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture.

However, applicant admitted prior art fails to discloses a planar /flat top surface, chemical machine polishing and insulation section. Although, it is well known in the art, as taught by Malazgirt.

In the same field of endeavor, Malazgirt discloses a method for manufacturing integrated circuits where the passivation film is planarized and where in the method comprises applying an SOG film and a forming another film over the SOG for forming the passivation section (col. 3, lines 10-30) to produce a substantial planarized surface. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant's admitted prior art, as taught by Malazgirt, since it would provide a planarized passivation layer which contributes to protection of the circuit and performance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fan et al (US 6,274,917) discloses a high efficiency color filter process for semiconductor array;

Ryu et al (US 5,908,672) discloses a method and apparatus for depositing a planarized passivation layer; and

De Santi et al. (EP 0887847 A1) discloses a process for final passivation of integrated circuit devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alicia M Harrington whose telephone number is 703 308 9295. The examiner can normally be reached on Monday - Thursday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 703 308 4883. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7724 for regular communications and 703 308 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

Alicia M Harrington Examiner Art Unit 2873

AMH 7 1 June 25, 2002

> Supervisory Patent Examiner Technology Center 2800